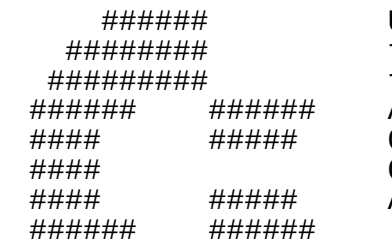
The original Commodore Business Machines PLUS/4 docs



Unfortunately, they were only available from http://www.plus4.org as large JPEG files so i started to translate them to ASCII.
Original Files donated by Tibor Biczo
Offered on the web by Mike Dailly
ASCII Version by Oliver Heun aka
The Paranoid / Paranoia

Absolutely no warranties are taken by the author of this textfile for the accuracy and correctness of this document nor about its legal status.
There are a lot of typos and misspellings in this text, but most are the original typos of the original Commodore docs which have not been corrected in this document.

Spellchecked, slightly edited and converted to PDF by Lidovski V., 2003

I. Scope

This document contains information concerning the architecture, hardware description, timing analysis, peripheral specification and driving software description for the Commodore system based on the 7360 I.C. (hereafter referred to as the TED I.C.) and the TED system. This document does not attempt to fully describe software aspects of the TED system and information concerning this subject can be found in the appropriate documents listed in section II.

1. System Overview

The TED system is based on the 7501 microprocessor, which is an HMOS version of the 6510, working in conjunction with the 7360 TED video processor. System RAM consists of 64K bytes of dynamic RAM composed of eight 648 X 1 devices. A system program is contained in two 16K X 8 ROMs, and in it's standard configuration, consists of Kernal and Basic version 3.5. The current implementation of the architecture for the Ted system supports up to 128K x 8 of ROM banked in 16K sections. ROM can be completely banked out and RAM banked in for a true 64K of RAM (minus two 256 byte pages). This allows 60,671 bytes available for Basic. The ROM/RAM banking is controlled by the 7360 under software control.

Keyboard scanning is done by outputting the row data on the Data bus while addressing a particular register in Ted, which will in turn cause Ted to latch the column information. Joystick scanning is done in the same manner.

Peripherals consist of standard serial bus products, (1541 disk drive, serial printer, etc.) cassette, TTL Serial ASCII which is intended to drive an RS-232 adapter. The expansion port supports ROM cartridges and a parallel disk drive interface.

SUMMARY OF TED SYSTEM FEATURES

- 7501 (6502 compatible) 8 bit CPU
- 7360 VLSI video, voice, DRAM controller
- 64KByte RAM
- 32KByte ROM for use in Kernal and Basic
- 32KByte ROM for Function Key software
- 32KByte ROM for Cartridge software
- Version 3.5 Basic with advanced graphics and DOS (compatible with C64)
- 40 X 25 display with 128 colors
- 320 X 200 graphics resolution
- 2 Voices and white noise
- 64 Keys including function keys
- Screen Editor with virtual Windows
- Dual speed system clock for increased processing throughput
- External power supply (same as c64)
- Low chip count, high system integration

2. SYSTEM ARCHITECTURE

The Ted system employs a shared bus concept which allows the video processor and the microprocessor to access the same memory and I/O devices on alternate halves of the system clock. Bus access control is generated by the 7360. To increase microprocessor throughput, when this interleaving is not needed, the system clock doubles in frequency and the microprocessor is allowed full time on the bus. This occurs when no video information is being fetched by the 7360 (horizontal or vertical retrace, blank screen). There is an exception to this, and that is when the 7360 DMA's the 7501 micro to accomplish attribute fetch and character pointer information.

Dynamic RAM control signals are generated by the 7360. /RAS is generated once each memory cycle, while /CAS is generated depending on whether the memory cycle is a DRAM memory cycle or not. MUX is generated to control the multiplex of Row and Column addresses going to the DRAMs. MUX also controls the holdoff of the R/W line as generated by the 7501. The R/W line is latched by the 7501 until the MUX line goes high signifying the end of the memory cycle. Refresh is provided by the 7360, refreshing 5 row locations (RAS only refresh) every raster line.

Selection of either ROM or RAM is accomplished by writing a bit in a TED register. When RAM is selected, the whole 64K memory map is comprised of RAM with the exception of 2 registers for the

7501 port, 1 page for TED control registers, and 1 page for I/O. This method yields 60.671 pages of RAM available for Basic program storage. When ROM is selected, the program residing in ROM appears in place of RAM. The exception to this is a write operation to ROM will always 'bleed through' to underlying RAM.

Kernal and Basic can also be selectively swapped out and replaced with other 16 K sections of ROM. 2 sockets are provided internally for application programs (referred to as function key software) and address space is allocated for 2 ROMs external to the system (cartridge use, etc.). Swapping is taken care of by a Kernal routine that does not swap out, (located at $FC00).

The cassette port and the Commodore serial bus port are implemented using the zero page ports available on the 7501 and using software control of hardware handshake.

The serial bus works with Commodore serial components, except for older peripherals that have a handshake timing problem.

The User Port is intended for external RS-232 adapters, and modem adapters. Transmission and reception is accomplished using a 6551 ACIA with handshaking assistance from a 6529 single port I.C.

The Joystick ports are functionally compatible with the standard Commodore 5 switch type joystick. They are not compatible with analog type peripherals such as paddles, tablets, etc., as well as not being pin compatible.

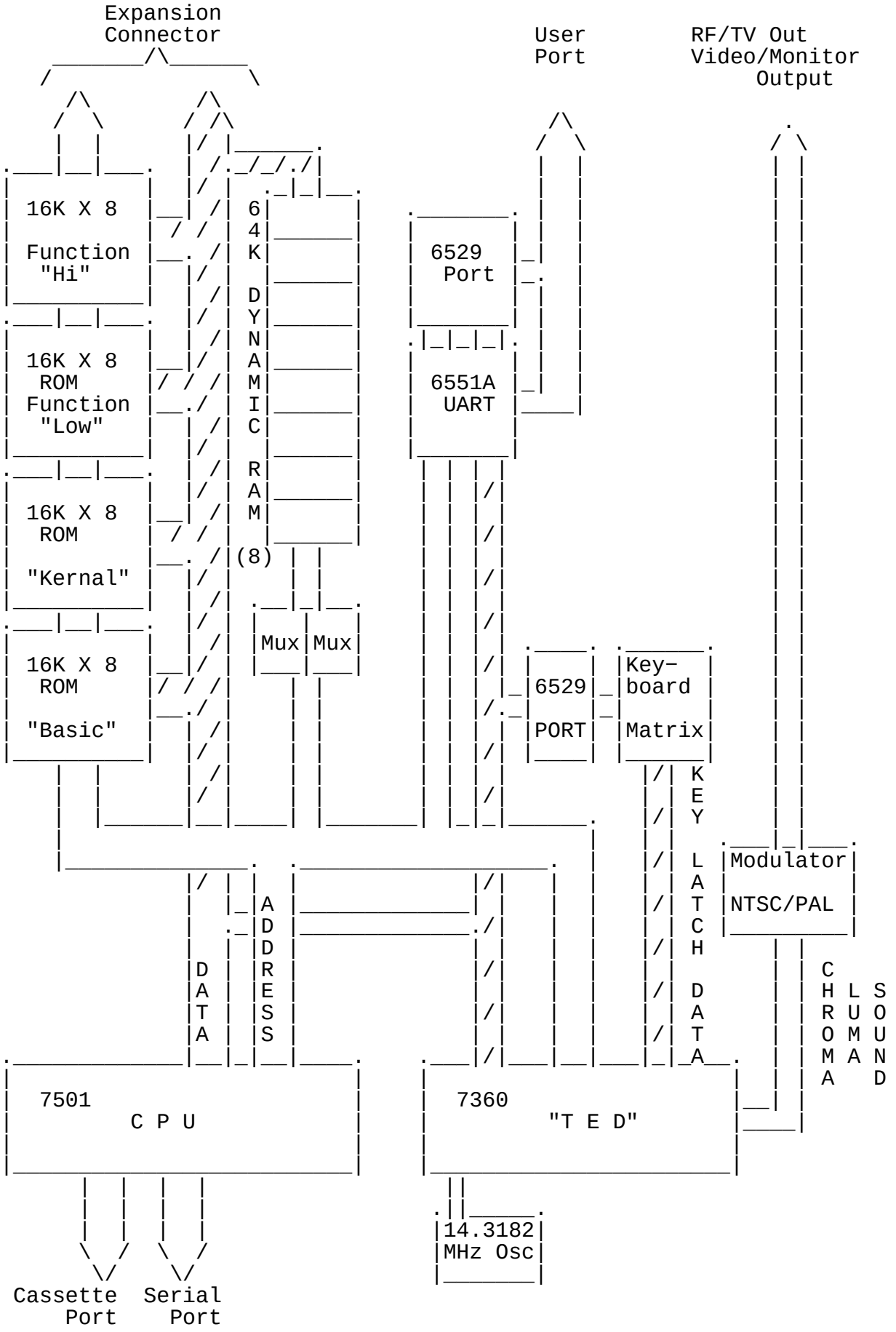
The video connector has composite video as well as separate chrome and luminance outputs for use with monitors. The 1701, 1702 type Commodore monitors interface directly to this connector.

The RF output Jack supplies an RF signal compatible with the resolutions pertaining to TV interface devices, and is switch selectable between channels 3 and 4. Both NTSC and PAL television standards are supported.

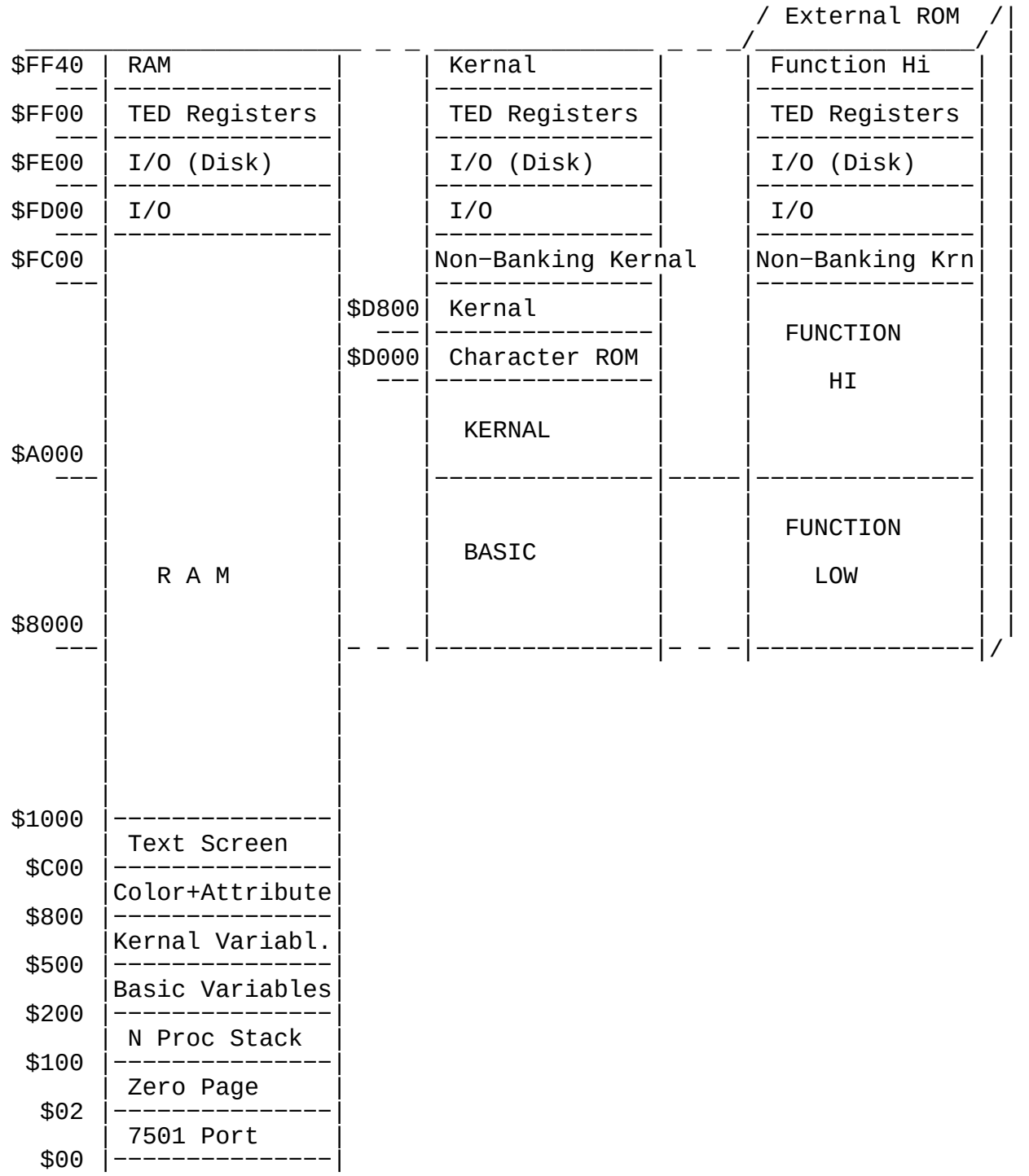
3. SYSTEM SPECIFICATIONS

This section covers the range of system operation by discussing various constraints and features of the TED system as a whole. Included are descriptions of the system as configured and limiting factors of power, loading, and environment.

3.1 TED 64 SYSTEM DIAGRAM



3.2 TED MEMORY MAP 64K



3.3 POWER CONSUMPTION

Part	I total (typ)	I total (max)		
7501	80	125	ma	
7360	200	250	ma	
23128	155	220	ma	Kernal, Basic
74LS257	24	38	ma	
modulator	80	150	ma	
555	10	15	ma	
7406	32	51	ma	
74LS08	4	9	ma	
74LS04	4	7	ma	
7700-xx	85	120	ma	
4164-2	336	480	ma	
6551A	34	60	ma	

6529B	56	80	ma	
6529B	56	80	ma	
	1156	1685	ma	W/O Function Key Soft
23128	155	220	ma	Function Key ROM
	1311	1905	ma	TED W/Function Soft
23128	155	220	ma	Cartridge ROM
	1466	2125	ma	TED64 Function and Cart
RS-232	1536	2225	ma	TED64 Func. w/Cart & RS-232

** 1.53 A Typ. 2.2 A Max.

3.4 BUS LOADING

Device	Address	Data	R/W	Ras Cas	
7501	12	15	12	-	pf
7360	10	10	10	10	pf
4164	-	20	80	80	pf
7700	8	-	-	8	pf
6551	10	10	10	-	pf
(2)6529	-	20	20	-	pf
74LS257	5	-	-	-	pf
(2)23128	16	16	-	-	pf
	61	91	132	98	pf *
	77	107	132	98	pf **
	93	123	132	98	pf ***

* TED64
** TED64 W/Function ROMs
*** TED64 W/Function & Cart

4 THE 7360 TEXT DISPLAY CHIP

This chapter will discuss the various aspects of the 7360 Text Display Chip.

4.1 OVERVIEW

The 7360 (or TED) is intended for low end 6502 family based personal home computers systems.s The 7360 is a 48 pin device which controls video output, (all signals are necessary to create composite video), system timing, dynamic RAM control, ROM control, and keyboard scanning. The 7360 contains 34 control registers which are accessed through the standard 6502 microprocessor data bus. The 7360 uses the MOS technology HMOS process, and is upgradable to HMOS 2.

4.2 FEATURES

Hardware features:

Dynamic RAM refresh

Sound generation

Programmable video time standards
(compatible with either NTSC or PAL standards)

40 column X 25 row character display

8 X 8 character dot matrix

320 X 200 pixel resolution

16 unique colors, 8 luminance levels

hardware flash

hardware cursor

hardware reverse video

programmable character information source (ROM or RAM)

dual speed clock

screen blanking for DMA sensitive environments

4.3 CHIP CHARACTERISTICS

This section discusses some of the physical characteristics of the TED chip.

4.3.1 PINOUT

Pin	Designation	Description
1	A2	Address Bit 2
2	A1	Address Bit 1
3	A0	Address Bit 0
4	VCC	Power Supply +5
5	CS0	Low ROM Chip Select
6	CS1	Hi ROM Chip Select
7	R/W	Read/Write Line
8	/IRQ	Interrupt Request
9	MUX	Address Multiplex Control
10	/RAS	Dynamic RAM Row Address Strobe
11	/CAS	Dynamic RAM Column Address Strobe
12	0OUT	System Clock
13	COLOR	Chroma Output
14	0IN	Master Clock
15	K0	Keyboard Latch 0
16	K1	Keyboard Latch 1
17	K2	Keyboard Latch 2
18	K3	Keyboard Latch 3
19	K4	Keyboard Latch 4
20	K5	Keyboard Latch 5
21	K6	Keyboard Latch 6
22	K7	Keyboard Latch 7
23	LUM	Composite Sync and Luminance
24	VSS	Power Supply Ground
25	DB0	Data Bit 0
26	DB1	Data Bit 1
27	DB2	Data Bit 2
28	DB3	Data Bit 3
29	DB4	Data Bit 4
30	DB5	Data Bit 5
31	DB6	Data Bit 6
32	DB7	Data Bit 7
33	SND	Sound Output
34	BA	Bus Available
35	AEC	Address Enable Control
36	A15	Address Bit 15
37	A14	Address Bit 14

38	A13	Address Bit 13
39	A12	Address Bit 12
40	A11	Address Bit 11
41	A10	Address Bit 10
42	A9	Address Bit 9
43	A8	Address Bit 8
44	A7	Address Bit 7
45	A6	Address Bit 6
46	A5	Address Bit 5
47	A4	Address Bit 4
48	A3	Address Bit 3

4.3.2 SIGNAL DESCRIPTION

Address Bus Pins 1 thru 3 and 36 thru 48

The 16 bit address bus is bidirectional. As an input, the microprocessor can access any of the 34 TED control registers. In the output mode TED uses the addresses to fetch Video Matrix Pointers, Attribute Pointers or character cell information. For microprocessor interface TED resides in locations FF00−FF3F in memory.

Data Bus Pins 25 thru 36

The 8 bit data bus is also bidirectional. The data bus activity can be separated into 2 categories: microprocessor interface and video data interface during the above mentioned fetches.

Keyboard latch Pins 15 thru 22

The 8 bit keyboard latch is used as the keyboard interface. Upon instruction by the microprocessor to write to the keyboard latch, the information on the keyboard pins is latched by the TED and stored until it is retrieved by the microprocessor on a read keyboard instruction. The 7360 also provides active pull ups on the keyboard matrix lines.

K0 and K1 (2 of the keyboard lines) also provide testing functions. When these pins are externally driven to 10 volts, they provide specific testing features. It should be noted however, that these pins are high impedance and if subjected to high energy electromotive fields, could cause false generation of testing functions. This can protected against through use of diodes to insure the potential K0 and K1 never exceeds VCC. K0 generates a system freeze function, and sets all horizontal flop−flops to force TED into dynamic RAM refresh period and single clock. All flip−flops are then released to allow their manipulation by the horizontal resistor. K1 forces the internal clock division into the NTSC mode.

Chip Selects Pins 5 and 6

TED generates ROM chip selects based on address decoding. CS0 is active during the memory block of 8000−BFFF (HEX). CS1 corresponds to C000−FFFF (HEX) in memory. The ROM area of memory can be banked out to overlay RAM, see the description of Registers 3E and 3F (HEX).

Dynamic RAM Control Pins 9 thru 11

TED generates /RAS and /CAS for dynamic RAM access. The signal MUX is also generated to externally multiplex the RAM row and column addresses.

Read/Write Pin 7

R/W is an input to TED to distinguish the type of operation to be performed. TED will actively pull up the system read line during all TED fetches. The read signal is qualified with MUX. The pin is an open source output.

Interrupt Pin 8

The interrupt pin is an open drain output. TED contains four interrupt sources: 3 internal timers and the raster comparator.

PHI Out Pin 12

For increased processor throughput, TED doubles the frequency of the system clock during horizontal and vertical blanking. The actual single clock boundaries are:

1) Raster lines 0−204 and horizontal positions 400−344
2) Horizontal positions 304−344

PHI In Pin 14

For use in NTSC television systems, TED requires a 14.31818 MHz +/− 70 ppm single phase clock input. For PAL systems, the input clock must be 17.734475 MHz +/− 70 ppm single phase.

Composite Color Pin 13

The color output contains all chrominance information, including the color reference burst signal and the color of all display data. The color output is open source and should be terminated with 1K ohms to ground.

Composite Sync and Luminance Pin 23

The luminance output contains all video synchronization as well as luminance information for the video display. The pin is open drain, required an external pullup of 1K Ohm.

Sound Pin 33

This pin provides the output of the 2 tone generators. The output must be integrated through an RC network and then buffered to drive an external speaker.

Bus Available Pin 34

Bus Available indicates the state of TED with respect to video memory fetches. BA will go low during phase 1, 3 single clock cycles before TED performs any memory access and will remain low for the entire fetch.

Address Enable Control Pin 35

During Double Clock mode, AEC is always high allowing the 7501 complete control of the system buses. For single clock time periods, when BA has not gone low, AEC will toggle with PHI2 out. This allows TED PHI1, time to complete its memory accesses of video dot information while the 7501 performs during PHI2. When TED needs both halves of the cycle to perform its customary PHI1 dot fetches and PHI2 attribute and pointer fetches, BA will go low. On the fourth PHI1 out, AEC will remain low until the end of the PHI2 video fetch.

4.4 ELECTRICAL SPECIFICATIONS

This section discusses some of the electrical properties and considerations of the 7360 TED chip.

4.4.1 ABSOLUTE MAXIMUM RATINGS

Input Voltage (Vin)	−2V to +7.0 VDC
Supply Voltage (Vcc)	−2V to +7.0 VDC
Operating Temp (Ta)	0 to 70 ’C
Storage Temp	−55 to 150 ’C
Input Leakage Current	−1.0 uA
Dynamic Characteristics	Vcc = 5.0V +/−5%
Input High Voltage (VIH)	Vss+2.4V to Vcc+1V
Input Low Voltage (VIL)	VSS−2V to VSS+.8V
Output High Voltage (VOL) (IOH=−200uA VCC=4.75VDC)	VSS+2.4V

Output Low Voltage (VOL) (IOL=−3.2ma VCC=5.25V)	VSS+.4V
Max Power Supply Current	250ma

4.4.2 VIDEO VOLTAGE SPECIFICATIONS

Chroma Out	1Vp−p min. w/2Volt Offset Open Source
Lum Out	0−5V (blanking = .5V) Open Drain

4.4.3 Luminance Levels (R7)

Level	Voltage
00	2.00 V
01	2.4 V
02	2.55 V
03	2.7 V
04	2.9 V
05	3.3 V
06	3.6 V
07	4.1 V
08	4.8 V

4.4.4 COLOR PHASE ANGLES

Color	HUE Phase (relative to SIN, in degrees) NTSC	PAL
Black	−−	−−
White	−−	−−
Red	70	103
Cyan	250	283
Magenta	20	53
Green	208	241
Blue	314	347
Yellow	134	167
Orange	90	129
Brown	115	148
Yllw−Grn	162	195
Pink	50	83
Blu−Grn	232	265
Lt−Blu	290	323
Dk−Blu	350	23
Lt−Grn	180	213

4.5 GENERAL TIMING

This section explores the various timing considerations and constraints related to the TED chip.

4.5.1 BUS TIMING

Parameter	Symbol	Min	Max	Unit
TED Addr Setup	TADS	−	150	ns
Input Data Setup	TDSU	50	−	ns
Input Data Hold	TDH	10	−	ns
Output Data Stable	TDSO	160	−	ns
Output Data Hold	TDHO	80	120	ns
R/W Stable Period	TRWS	−	178	ns
MUX to R/W Setup	TMRWS	−	70	ns
MUX to R/W Hold	TMRWH	30	−	ns
Chip Select Setup	TCSS	−	320	ns
Chip Select Hold	TCSH	70	−	ns
Address Hold	TAH	60	−	ns

Address in Tristate	TADTH	– 135	ns

4.5.2 DMA TIMING

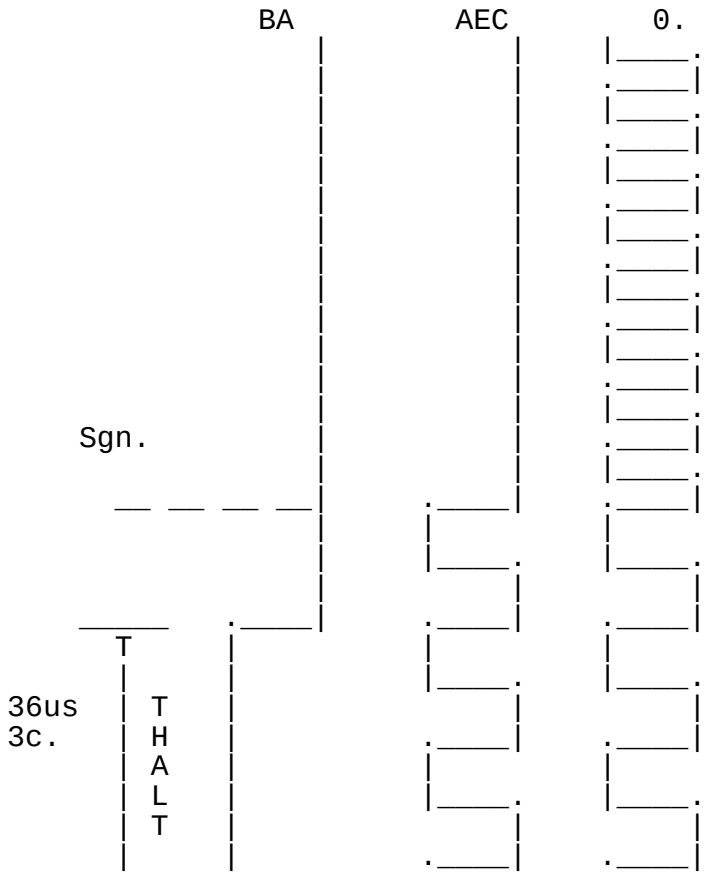
The 7360 performs DMA’s to fetch additional information to maintain a video display. Twice per each row of characters, (a character being defined as a cell 8 X 8 bits) to obtain the attributes for each character and to obtain the character pointer which points to where the character pattern can be found. In bit map mode, these DMA’s still occur, but the information is interpreted differently. The sequence of events in a DMA cycle are: 1)The system clock comes out of double speed for 1 cycle. At the same time AEC starts to toggle, allowing the 7360 on the bus. 2)The Bus Available line goes low. 3)Three cycles are given to the 7501 to complete operation before DMA begins. 4)40 cycles of single clock where the 7360 is doing 2 fetches per cycle. 5)BA goes high at the same time as AEC allowing the 7501 back on the bus. 6)5 cycles follow of single speed where the 7360 is engaged in refreshing the dynamic RAM. 7)16 cycles of double speed – (equiv. to 8 cycles of single) 8) If last DMA was row 8 of character, then DMA for row 1 of next character is initiated. If screen is blanked, the 5 cycles of single speed are still present for dynamic RAM refresh.

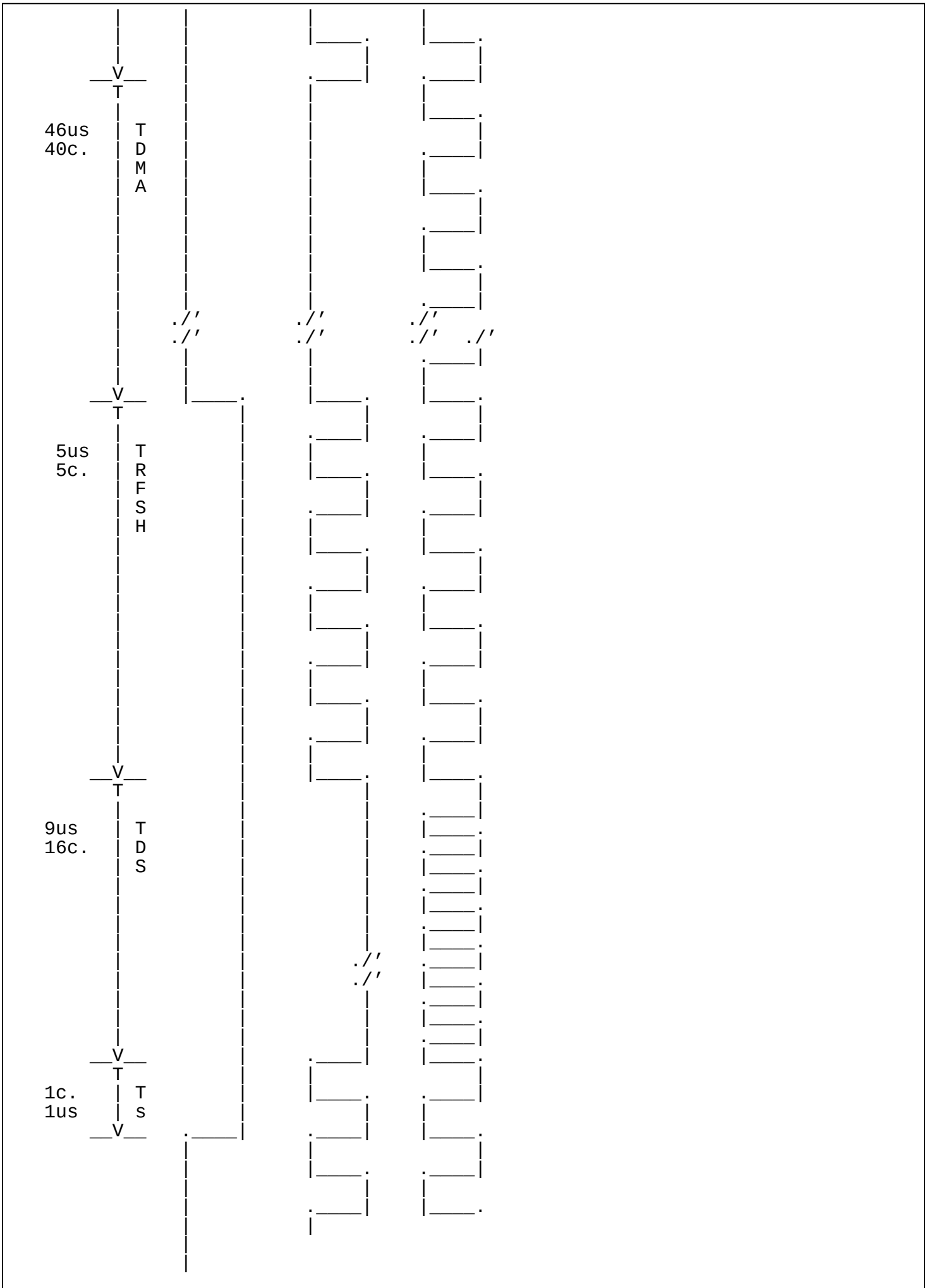
4.5.2.1 TED DMA TIMING (REFER TO 4.5.2.2 TED DMA TIMING DIAGRAM)

	cycles	time	
THALT	3	3us	Time, Halt
TDMA	40	46us	Time, DMA
TRFSH	5	5us	Time, Refresh
TDS	16	9us	Time, Double Speed
TS	1	1us	Time, Synchronize
	65	64us	

Diagram 4.5.2.2 represents the occurrence of when two DMAs are ’back to back’. I.E. character row 8 DMA’s, then character row 1 of the next character DMAs, separated only be one horizontal retrace.

4.5.2.2 TED DMA TIMING DIAGRAM




46us
40c.
TDMA
5us
5c.
TRFSH
9us
16c.
TDS
1c.
1us
Ts

5 THE 7501 MICROPROCESSOR

This section describes some of the properties and functions of the type 7501 microprocessor.

5.1 7501 DESCRIPTION

The 7501 is an HMOS version of the 6502 family or more specifically, the 6510CBM. The 7501 is software compatible with existing 6502, 6510 code. The 7501 contains a 7 bit bi−directional port used to directly drive the serial bus and cassette. The port is at location $0000 while the data direction register is at $0001. The 7501 is Tri−statable and through use of the AEC (address enable control) line and is used extensively in the TED shared bus concept. DMA is accomplished using the AEC line and the RDY line (called BA on TED). A control line is provided (GATE IN) to hold off the R/W line until /RAS makes the transition from low to hi. This prevents the Real line from making an early transition to the write state which would cause an improper Early Write Cycle to occur.

5.2 7501 PINOUT

Pin	Name	Description
1	PHI In	System Clock Input
2	RDY	DMA Rqst
3	/IRQ	Interrupt Rqst
4	AEC	Address Enable Control
5	VCC	Power Supply +5V.
6	A0	Address Bit 0
7	A1	Address Bit 1
8	A2	Address Bit 2
9	A3	Address Bit 3
10	A4	Address Bit 4
11	A5	Address Bit 5
12	A6	Address Bit 6
13	A7	Address Bit 7
14	A8	Address Bit 8
15	A9	Address Bit 9
16	A10	Address Bit 10
17	A11	Address Bit 11
18	A12	Address Bit 12
19	A13	Address Bit 13
20	GND	Power Supply Ground
21	A14	Address Bit 14
22	A15	Address Bit 15
23	GATE In	R/W Gate
24	P7	Port Bit 7
25	P6	Port Bit 6
26	P4	Port Bit 4
27	P3	Port Bit 3
28	P2	Port Bit 2
29	P1	Port Bit 1
30	P0	Port Bit 0
31	DB7	Data Bit 7
32	DB6	Data Bit 6
33	DB5	Data Bit 5
34	DB4	Data Bit 4
35	DB3	Data Bit 3
36	DB2	Data Bit 2
37	DB1	Data Bit 1
38	DB0	Data Bit 0
39	R/W	Read/Write
40	RES	Reset

5.3 7501 ELECTRICAL SPECIFICATIONS

This section describes some of the electrical

constraints and specifications of the system.

5.3.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	−0.3 to +7.0	Vdc
Input Voltage	Vin	−0.3 to +7.0	Vdc
Operating Temperature	Ta	0 to +70	C
Storage Temperature	Tstg	−55 to +150	C

5.3.2 ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	VIH				
Phi0(in)		Vss+2.4	---	Vcc	Vdc
/RES,P0−P7,/IRQ,Data		Vss+2.2	---	---	Vdc
Input Low Voltage	VIL				
Phi0(in)		Vss−0.3	---	Vss+0.5	Vdc
/RES,P0−P7,/IRQ,Data		---	---	Vss+0.8	Vdc
Input Leakage Current (Vin=0 to 5.25V, Vcc=5.25V)	Iin				
Logic		---	---	2.5	uA
Phi0(in)		---	---	10.0	uA
3−State(Off) Inp.Cur. (Vin=0.4 to 2.4V, Vcc=5.25V)	ITSI				
Data Lines		---	---	10.0	uA
Output High Voltage (IOH=−100uAdc, Vcc=4.75V)	VOH				
Data,A0−A15,R/W,P0−P7		Vss+2.4	---	---	Vdc
Output Low Voltage, (IOL=1.6mADC, Vcc=4.75V)	VOL				
Data,A0−A15,R/W,P0−P7		---	---	Vss+0.4	Vdc
Power Supply Current	ICC	---	125	---	mA
Capacitance (Vin=0,Ta=25 C, _ f=1MHz)	C				
Logic,P0−P7	Cin	---	---	10	pF
Data	Cout	---	---	15	pF
A0−A7	Cout	---	---	12	pF
Phi1	CPHi1	---	30	50	pF
Phi2	CPHi2	---	50	80	pF

5.4 SIGNAL DESCRIPTION

CLOCK (PHI 0) − This is the dual speed system clock and is a standard TTL level input.

ADDDRESS BUS (A0 − A15) − TTL output. Capable of driving 2 TTL loads at 130 pf.

DATA BUS (D0 − D7) − Bi−directional bus for transferring data to and from the device and the peripherals. The outputs are tri−state buffers capable of driving 2 standard TTL loads and 130pf.

RESET − This input is used to reset or start the processor from a power down condition. During the time that this line is held low, writing to or from the processor is inhibited. When a positive edge is detected on the input, the processor will immediately begin the reset sequence. After a system initialization time of 6 cycles, the mask interrupt flag will be set and the processor will load the program counter from the contents of memory locations $FFFC and $FFFD. This is the start location for

program control. After VCC reaches 4.75 Volts in a power up routine, reset must be held low for at least 2 cycles. At this time the R/W line will become valid.

INTERRUPT REQUEST (IRQ) − TTL input, request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. At that time, the interrupt mask in the Status Code Register will be examined. If the interrupt mask is not set, the processor will begin an interrupt sequence. The Program Counter and the Processor status register will be stored on stack and the interrupt disable flag is set so that no other interrupts can occur. The processor will then load the program counter from the memory locations $FFFE and $FFFF.

ADDRESS ENABLE CONTROL (AEC) − The Address Bus is only valid when the AEC line is high. When low, the address bus is in a high impedance state. This allows easy DMA's for shared bus systems.

I/O PORT (P0−P4,P6,P7) − Bidirectional port used for transferring data to and from the processor directly. The Data Output Register is located at location $0001 and the Data Direction Register is located at location $0000.

R/W − TTL level output from processor to control the direction of data transfer between the processor and memory, peripherals, etc. This line is high for reading memory and low for writing. This line is latched by the Gate In line to synchronize between a DRAM memory cycle and the processor clock cycle. If AEC is low when Gate In makes a low to high transition, the R/W line will go to a high impedance until the next transition of the Gate In line and AEC is high prior to the transition.

GATE IN − TTL level input, used to gate the R/W line to prevent the R/W line from going low during a read cycle, before RAS and CAS so high (resulting in a Read/Write cycle). Normally connected to the MUX line in a system configuration to synchronize the DRAM memory cycle to the processor clock cycle.

RDY − Ready. TTL level input, used to DMA the 7501. The processor operates normally while RDY is high. When RDY makes a transition to the low state, the processor will finish the operation it is on, and any subsequent operation if it is a write cycle. On the next occurrence of read cycle the processor will halt, making it possible to tri−state the processor to gain complete access to the system bus.

5.5 PROCESSOR TIMING

This section explores the timing considerations of the 7501 processor unit.

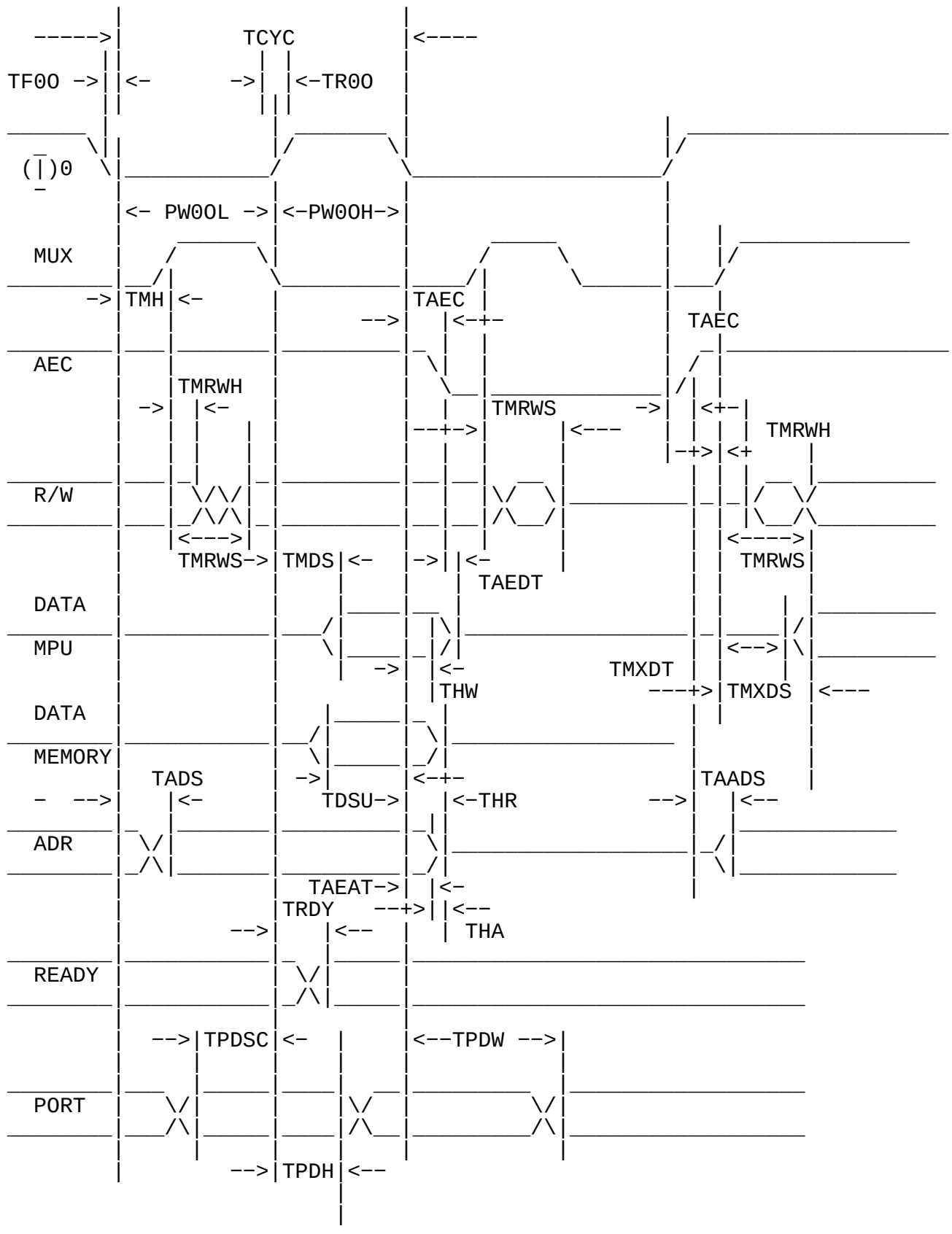
5.5.1 TIMING CHART

Electrical Characteristics Vcc = 5v + 5%, Vss = 0v, TA = 0 °C to 70 °C

Characteristic	Symbol	Min	Max	Units
MUX input high	TMH	60	110	ns
AEC setup time	TAEC	25	60	ns
MUX to RW setup or tri−state	TMRWS		70	ns
MUX to RW hold	TMRWH	30		ns
Up data setup from PH0	TMDS		130	ns
Up write data hold	THW	60		ns
Up data setup from Mux	TMXDS		120	ns
Data bus to tri−state from MUX	TMXDT	30		ns
Data bus to tri−state from AEC	TAEDT		120	ns
Read data stable	TDSU	40		ns
Read data hold	THR	40		ns
Address setup from PH0	TADS	40	150	ns
Address hold	THA	40		ns
Address setup from AEC	TAADS		75	ns
Address tri−state from AEC	TAEAT		120	ns
Port input setup	TPDSU	105		ns

Port input half	TPDH	65		ns
Port output data valid	TPDW		195	ns
Cycle time	TCYC	500		ns
PH0(in) pulse width @1.5v	PWHPH0	250	275	ns
PH0(in) rise time	TRPH0		10	ns
PH0(in) fall time	TFPH0		10	ns
RDY setup time	TRDY	80		ns

5.5.2 TIMING DIAGRAM



6. DYNAMIC RAMS

This chapter covers the constraints and features of dynamic random access memories used in the TED system.

6.1 ELECTRICAL SPECIFICATIONS

Input Voltage (Vin)	−1V to +7.0 VDC
Supply Voltage (Vcc)	−1V to +7.0 VDC
Operating Temp (Ta)	0 to 70 ’C
Storage Temp	−55 to 150 ’C
Input Leakage Current	−10.0 uA
Dynamic Characteristics	Vcc = 5.0V +/−5%
Input High Voltage (VIH)	Vss+2.4V to Vcc+1V
Input Low Voltage (VIL)	VSS−1V to Vss+.8V
Output High Voltage (VOH) (IOH=−200uA VCC=4.75VDC)	VSS+2.4V
Output Low Voltage (VOL) (IOL=−4.2ma VCC=5.25V)	VSS+.4V
Max Power Supply Current	80ma

6.2 CHARACTERISTICS

This section covers some of the characteristics of the 64K by 1 bit RAM that is used in the TED 64 system.

6.2.1 PACKAGE PINOUT

PIN	NAME	DESCRIPTION
1	NC	
2	Din	Data in
3	/WE	Write Enable (Active Low)
4	/RAS	Row Address Strobe (Active Low)
5	A0	Address Bit 0
6	A2	Address Bit 2
7	A1	Address Bit 1
8	VCC	Power Supply +5
9	A7	Address Bit 7
10	A5	Address Bit 5
11	A4	Address Bit 4
12	A3	Address Bit 3
13	A6	Address Bit 6
14	Dout	Data Out
15	/CAS	Column Address Strobe (Active Low)
16	VSS	Power Supply Ground

6.2.2 SELECTION CRITERIA

The TED system uses low cost 200 ns access RAMs. Qualified parts must meet all timing parameters as specified in section 6.3.1 ’TIMING CHART’ and 6.3.2 ’TIMING DIAGRAM’.

6.3 TIMING

This section illustrates the required timing constraints in dealing with DRAM.

(The next 2 scans [32,33] depicting the RAM timing chart are definitely unreadable and therefore missing)

7. THE USER PORT

This chapter details the system User Port.

7.1 DESCRIPTION

The USER PORT is included to allow various terminal and modem devices to connect to the TED system. Transmission and reception is via a 6551 ACIA, with handshaking assistance from a 6529 single port device. The 6551 and the 6529 are each accessible to the TED system in software, thus allowing their programming for various applications.

The 6551 ACIA is enabled by addresses $FD00 to $FD0F. The least significant two bits of the address will choose the mode, which may be set for transmit/receive, receive status, or programming of either the command register or the control register. Similarly, the 6529 is activated by the addresses $FD10 to $FD1F. It permits seven bits of either input or output, depending upon the status of the Read/Write line. The eighth bit, bit two to be exact, is used as the cassette sense input. It may be possible to utilize this bit of certain precautions are taken in software. (I.E. Insure that cassette sense is not grounded.)

The User Port itself provides access to various signals generated by these two chips, in addition to the ATN and Buffered Reset (BRESET) lines of the TED system. The port also provides ground, +5VDC and +9VAC for use by connected devices.

7.2 PHYSICAL PINOUT

PIN	NAME	DESCRIPTION	DIRECTION
A	GND	Ground	---------
B	P0	I/O Port Bit 0	Input/Output
C	RxD	Receive Data	Input
D	RTS	Request to Send	Output
E	DTR	Data Terminal Ready	Output
F	P7	I/O Port Bit 7	Input/Output
H	DCD	Data Carrier Detect	Input
J	P6	I/O Port Bit 6	Input/Output
K	CTS	Clear to Send	Input
L	DSR	Data Set Ready	Input
M	TxD	Transmit Data	Output
N	GND	Ground	----------
1	GND	Ground	----------
2	+5	+5VDC	----------
3	/BRESET	Buffered System Reset	Output
4	P2/CST Sense	I/O Port Bit 2	Input/Output
5	P3	I/O Port Bit 3	Input/Output
6	P4	I/O Port Bit 4	Input/Output
7	P5	I/O Port Bit 5	Input/Output
8	RxC	Receive Clock	Input/Output
9	ATN	Attention	Output
10	+9	+9 VAC	----------
11	+9	+9 VAC	----------
12	GND	Ground	----------

7.3 ELECTRICAL SPECIFICATIONS

I/O Ports (P0,P2..P7)

These ports are capable of driving up to four TTL type loads each in output configuration.

Buffered Reset (/BRESET)

The buffered reset line is capable of driving at least one TTL level load. It can drive a total of ten TTL loads

between the User Port, the Serial Port, and the Expansion Port.

Attention (ATN)

This line is capable of driving at least one TTL level load. It can drive a total of ten TTL loads between the User Port and the Serial Port.

Receive Data (RxD)

The Receive Data input may be driven by a single TTL level driver.

Other Inputs (DCD, DSR, CTS)

The remaining data inputs are buffered by TTL buffers. Each may be driven by a single TTL level driver. CTS is sensed via 6529 under software control.

Receive Clock (RxC)

The Receive Clock, when acting as an output, can drive a single TTL level load. As an input, it must be driven by at least one TTL level load.

Transmit Data (TxD)

The Transmit Data output is capable of driving a single TTL level load.

Other Outputs (RTS, DTR)

The remaining outputs are each buffered by a TTL buffer, thus each of them will drive ten TTL level loads.

Five volt source (+5)

The five volt source is regulated DC, capable of supplying 100 mA worst case.

Nine volt source (+9)

The nine volt source is an unregulated nine volt (RMS) supply, capable of supplying a worst case current of 400 DC mA.

7.4 TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT
Transmit/Receive Clock Rate	Tccy	400	–	ns
Transmit/Receive Clock High Time	Tch	175	–	ns
Transmit Receive Clock Low Time	Tcl	175	–	ns
XTAL1 to TxD Propagation Delay	Tdd	–	500	ns
Propagation Delay (/RTS, /DTR)	Tdly	–	500	ns
/IRQ Propagation Delay (Clear)	Tirq	–	500	ns

(The next 3 diagrams [in the 37 scan] depicting the

User port timing are too tiny to read and have been skipped)

7.5 6551, 6529 TIMING

PARAMETER	SYMBOL	MIN	MAX	UNIT
PHI 2 PW	PW02	248	350	ns
Address Set Up Time	TACR TACW	72	–	ns
Address Hold	TCAH TCAR	25	–	ns
R/W Setup	TWCW TWCR	71	–	ns
R/W Hold	TCWH TWCR	93	–	ns
Data Bus Setup	TDCW	148	–	ns
Read Access	TCDR	195	–	ns
Read Data Hold	THR	35	–	ns

(The following two diagrams, Write Cycle and Read Cycle [in the 38 scan] are too tiny to read and have been skipped)

7.6 PLA PROGRAM CHART

	PRODUCT TERM					ACTIVE LEVEL							
	INPUT VARIABLE												
N													
U	1	1	1	1	1	1							
M	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	H	H	L	L	L	L	H	L
													OUTPUT FUNCTION											
													7	6	5	4	3	2	1	0				
0	–	–	–	–	–	–	–	H	–	–	–	–	–	–	–	–	A	.	.	.	.	.	.	.
1	L	–	–	–	–	–	–	–	–	–	–	–	–	–	H	H	A	.	.	.	.	.	A	.
2	–	H	H	H	L	H	H	–	H	L	L	L	L	H	H	–	.	.	.	.	A	.	.	.
3	L	H	H	H	L	H	H	–	H	L	L	L	H	H	H	H	.	.	.	.	.	A	.	.
4	L	H	H	H	L	H	H	–	H	L	L	H	H	H	H	H	.	.	A	.	.	.	.	.
5	–	H	H	H	L	L	H	–	H	–	–	–	–	H	–	–	.	A	.	.	.	.	.	.
6	L	H	H	H	L	H	H	–	H	H	H	L	H	H	H	H	.	.	.	A	.	.	.	.
7	L	H	H	H	L	H	H	–	H	L	L	H	L	H	H	–	.	.	.	.	.	.	.	A

___A10	A13	A8 MUX	A7	A5	A15	F7	
RAS	A11	A9	A14	A12	A6	A4	Ph0

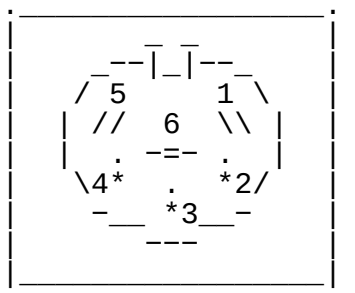
A	K	K	A	6	6	P	S
R	E	E	D	5	5	H	P
M	R	Y	D	5	2	I	E
	N	P	R	1	9	2	E
		O					C
		R	C	$	$	C	H
		T	L	F	F	L	
			K	D	D	K	$
			$		0	1	F
			F	$	X	X	D
			D	F			2
			3	D			X
			X	D			
				X			

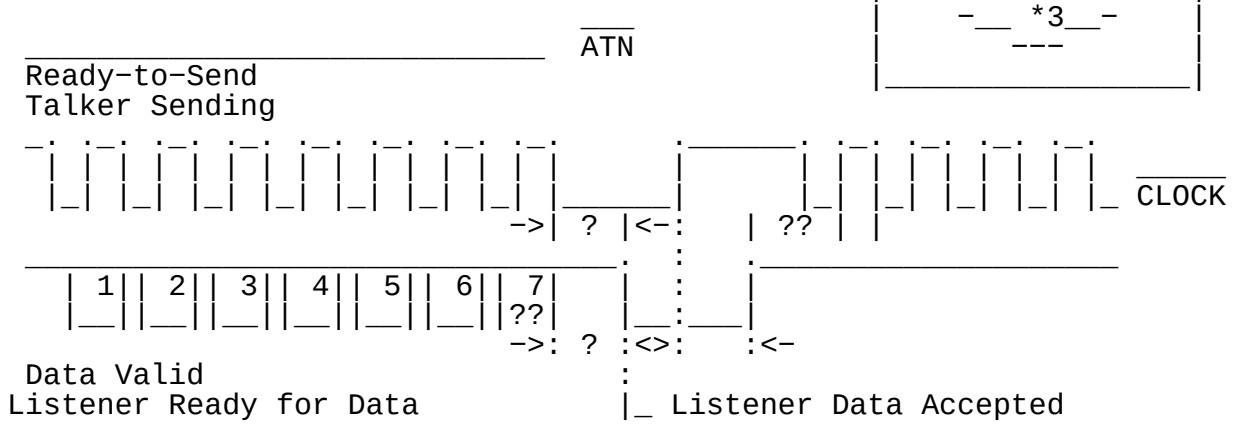
(7.7 TED PHI 2 Generation and
  PLA Internal Logic [40th scan]
  are hard to turn to ASCII and
  partly too tiny to read   )

9. THE SERIAL BUS

9.1 SERIAL BUS SPECIFICATION
9.2 SERIAL BUS CONNECTOR PINOUT

Pin	Type
1	Serial SRQIN
2	GND
3	SERIAL ATN IN/OUT
4	SERIAL CLK IN/OUT
5	SERIAL DATA IN/OUT
6	RESET





SERIAL BUS TIMING

	Symbol	Min	Typ	Max
ATN Response (Required) (1)	TAT	–	–	1000us
Listener Hold-Off	TH	0	–	oo
Non-EOI Reponse to ??? (2)	TNE	–	40ns	200us
Bit Set-Up Talker (4)	TS	20us	70us	–
Data Valid	TV	20us	20us	–
Frame Handshake (3)	TF	0	20	1000us
Frame To Release to ATN	TR	20us	–	–
Between Bytes Time	TBB	100us	–	–
EOI Response Time	TYE	200us	250us	–
EOI Reponse Hold Time (5)	TE	60us	–	–
Talker Response Limit	TRY	0	30us	60us
Byte Acknowledge (4)	TPR	20us	30us	–
Talk Attention Release	TTK	20us	30us	100us
Talk Attention Acknowl-DOS	TDC	0	–	–
Talk Attention Ack.Hold	TDA	50us	–	–
EOI Acknowledge	TFR	60us	–	–

(5) TEI Min. Must be 80us for external device to be a Talker
(4) TV and TPR min must be 60us for external device to be a Talker

(3) If Max. Time exceeded, Frame Error.
(2) If Max. Time exceeded EOI Response required
(1) If Max. Time exceeded, Device not present Error

Notes:

(Both diagrams and table are partly hand-written and are hard to read. Some of the times might be ms instead of us, some of the labels might be wrong)

10. THE EXPANSION BUS

10.1 EXPANSION BUS PINOUT

PIN	NAME	PIN	NAME
1	GND	A	GND
2	+5	B	C1LOW
3	+5	C	/BRESET
4	/IRQ	D	/RAS
5	R/W	E	PHI0
6	CIHI	F	A15
7	C2LOW(reserved)	H	A14
8	C2HI(reserved)	J	A13
9	/CS1	K	A12
10	/CS0	L	A11
11	/CAS	M	A10
12	MUX	N	A9
13	BA	P	A8
14	D7	R	A7
15	D6	S	A6
16	D5	T	A5
17	D4	U	A4
18	D3	V	A3
19	D2	W	A2
20	D1	X	A1
21	D0	Y	A0
22	AEC	Z	NC
23	EXT AUDIO	AA	NC
24	PHI 2	BB	NC
25	GND	CC	GND

10.2 EXPANSION CONNECTOR SIGNAL DESCRIPTION

A0 − A15	System Address Bus − unbuffered, Output.
D0 − D7	System Data Bus − unbuffered. Output.
/CS0,/CS1	Internal ROM Chip Selects. Output.
/C1LOW, C1HI	External Cartridge Chip Selects. Active Low. Output.
/RAS	DRAM Row Address Strobe. Output.
MUX	DRAM Address Multiplex Control Signal. Output.
/CAS	DRAM Column Address Strobe. Output.
BA	Bus Available. Low for DMA. Output Only.
PHI 2	Artificial PHI 2. Address Valid Rising Edge. Data Valid Falling Edge. Output.
R/W	System Read Write Line. Output.

/IRQ Interr. Request. Input.

/BRESET Buffered Reset. Output.

EXT AUDIO External Audio. Input. 1 V p–p Full Scale. AC Coupled.

11. READ ONLY MEMORY

11.1 SYSTEM ROM DESCRIPTION

In a basic configuration, the TED operating system resides in 32K of read only memory contained in two 16K X 8 ROM. The KERNAL resides in the upper 16K ROM (referred to as High ROM) and some of the lower 16K ROM (LOW ROM). The Kernal, by definition, is the operating system of the computer, with fixed entry points into usable subroutines to facilitate use by higher level programs. The entry table for the Kernal is located above the 7360 in memory. ($FF40 – $FFF9) Contained in the space allocated for the Kernal is the character ROM at location $D000 – $D7FF. 'BASIC' is contained in the lower ROM not used by the Kernal.

11.2 BANKING ROM OPERATION

Although the system can only 'see' 32K of ROM at a time, up to 64K can be installed on bpard, with an additional 32K on as external cartridge. This is possible using the scheme known as 'banking'. Banking is accomplished by writing to three address range of $FDD0 – $FDDF. When a write to this address range occurs, the lower four bits of the address bus select 2 of 8 banks (each 16K). Refer to the chart below.

A0	A1	BANK
0	0	low internal #1, 'BASIC'
0	1	low internal #2, 'FUNCTION LOW'
1	0	low external #1, 'CARTRIDGE LOW'
1	1	reserved

A2	A3	BANK
0	0	hi internal #1, 'KERNAL'
0	1	hi internal #2, 'FUNCTION HI'
1	0	hi external #1, 'CARTRIDGE HI'
1	1	reserved

Even when the Kernal is banked out, part of the Kernal remains accessible. This is the part of the Kernal that does the actual banking and is located in the address range of $FC00 to $FCFF. This section of ROM will not assert itself if ROM is banked out for RAM.

11.3 ROM ELECTRICAL SPEC

Absolute Maximum Ratings

INPUT VOLTAGE (Vin) –.5V to +7.0 VDC

SUPPLY VOLTAGE (Vcc)	−.5V to +7.0 VDC
OPERATING TEMP (Ta)	0 to 70 ’C
STORAGE TEMP	−55 to 150 ’C

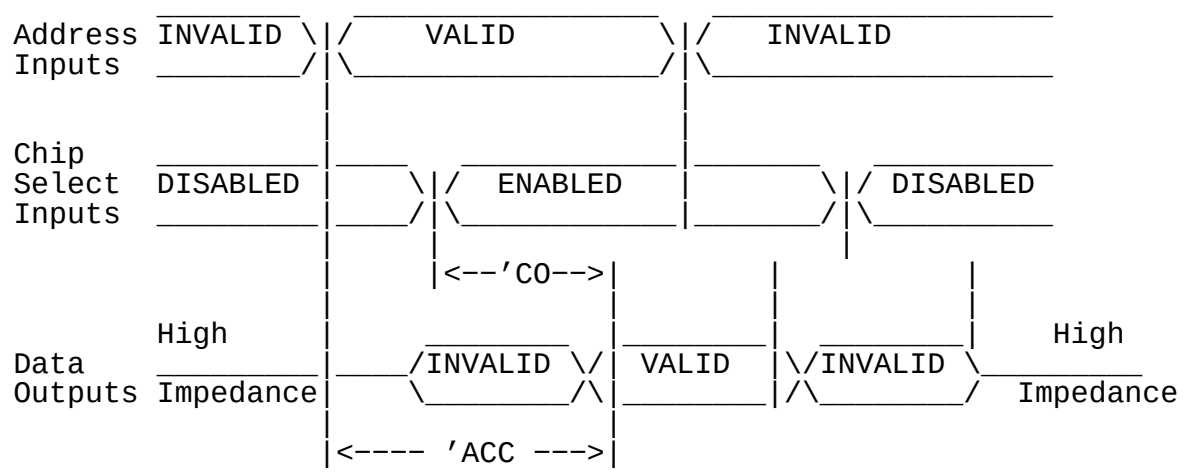
D.C. Characteristics

INPUT LEAKAGE CURRENT	−10 ua
DYNAMIC CHARACTERISTICS	Vcc = 5.0V +/−5%
INPUT HIGH VOLTAGE (VIH)	Vss+2.4V to Vcc+1V
INPUT LOW VOLTAGE (VIL)	VSS−.5V to Vss+.8V
OUTPUT HIGH VOLTAGE (VOH) (IOH=−200uA VCC=4.75VDC)	VSS+2.4V
OUTPUT LOW VOLTAGE (VOL) (IOL=−3.2ma VCC=5.25V)	VSS+.4V
MAX POWER SUPPLY CURRENT	120 mA

11.4 23128 ROM PINOUT

PIN	NAME	DESCRIPTION
1	NC	
2	A12	Address Bit 12
3	A7	Address Bit 7
4	A6	Address Bit 6
5	A5	Address Bit 5
6	A4	Address Bit 4
7	A3	Address Bit 3
8	A2	Address Bit 2
9	A1	Address Bit 1
10	A0	Address Bit 0
11	D0	Data Bit 0
12	D1	Data Bit 1
13	D2	Data Bit 2
14	GND	Power Supply Ground
15	D3	Data Bit 3
16	D4	Data Bit 4
17	D5	Data Bit 5
18	D6	Data Bit 6
19	D7	Data Bit 7
20	/CS	Chip Select / Active Low
21	A10	Address Bit 10
22	/CE	Chip Enable / Active Low
23	A11	Address Bit 11
24	A9	Address Bit 9
25	A8	Address Bit 8
26	A13	Address Bit 13
27	CS or CE	Chip Select or Chip Enable / Active High
28	VCC	Power Supply +5

11.5 ROM TIMING SPECIFICATION



PARAMETER	SYMBOL	MIN.	MAX.	
ACCESS TIME	TACC	300	–	ns
OUTPUT ENABLE	TOE	120	–	ns

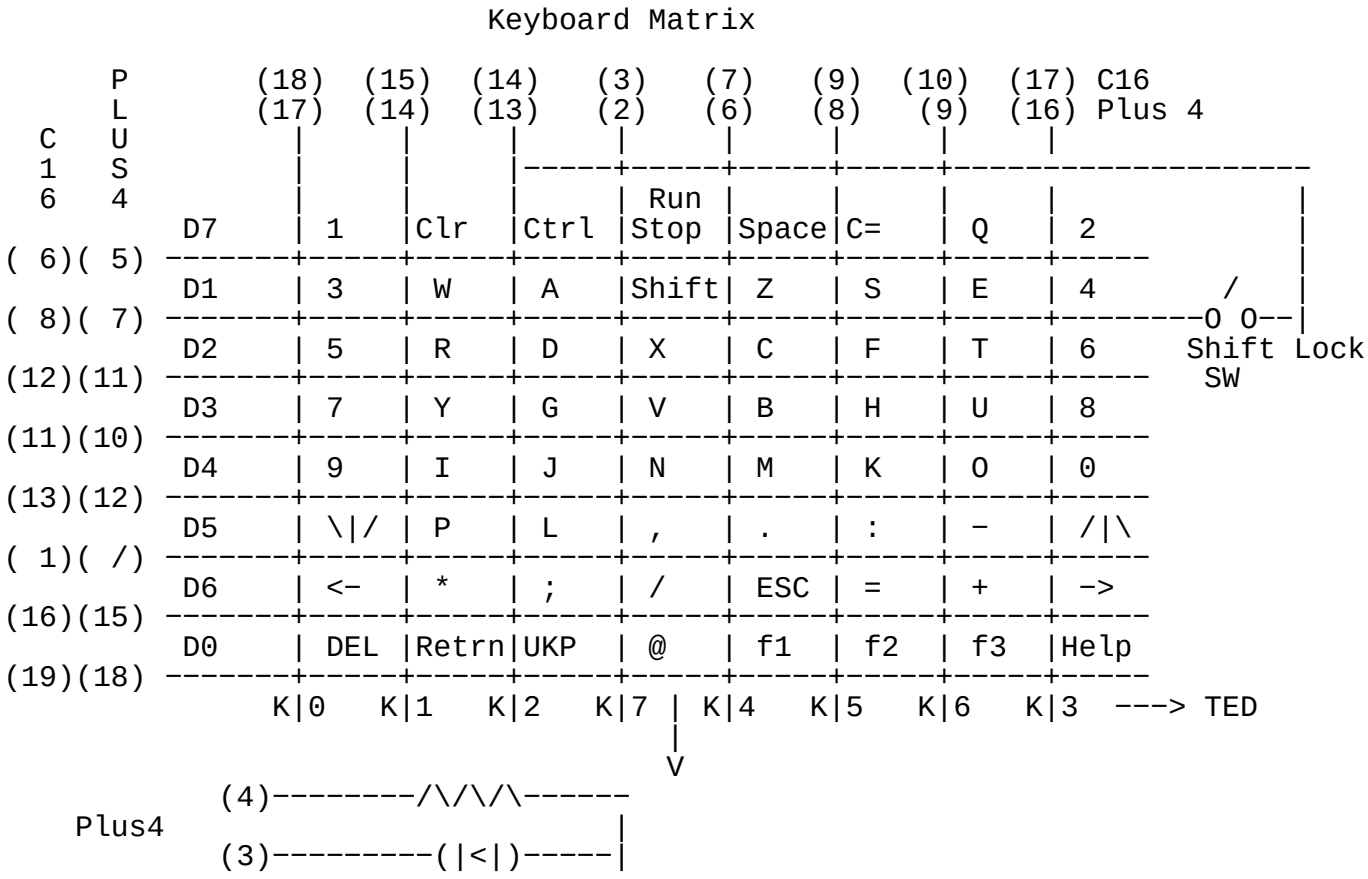
Note: TACC available from system is 338ns and TOE available is 12

12. THE KEYBOARD

12.1 KEYBOARD CONNECTOR PINOUT

PIN		NAME	DESCRIPTION
1	1	D5	Data Bit 5
1	3	K7	Key Latch Bit 7
3	4	GND	LED GND
4	–	+5V	LED +5Volt 20ma Max.
5	6	D7	Data Bit 7
6	7	K4	Key Latch Bit 4
7	8	D1	Data Bit 1
8	9	K5	Key Latch Bit 5
9	10	K6	Key Latch Bit 6
10	11	D3	Data Bit 3
11	12	D2	Data Bit 2
12	13	D4	Data Bit 4
13	14	K2	Key Latch Bit 2
14	15	K1	Key Latch Bit 1
15	16	D6	Data Bit 6
16	17	K3	Key Latch Bit 3
17	18	K0	Key Latch Bit 0
18	19	D0	Data Bit 0

12.2 KEYBOARD MATRIX (Plus4 C16)



12.3 KEYBOARD ELECTRICAL SPECIFICATION

1) Maximum Rating — 12VDC, 200uS pulse width 1/50 duty cycle 1ma

2) Chattering — 5mSEC Initial, 10mSEC over life

3) Contact Resistance — 500 Ohm max.

4) Capacitance — 100pf max.

5) Insulation res. — 50M Ohm min.

6) Withstand voltage — 250VAC 1min.

7) Operating force — 65s typ.

Zero trav force 15+/−10g at .5mm trav

Full trav force 90+/−25g at .5mm above full trav

8) Operating life — 500 million times
Function keys — 300 million times

9) Operating Temp — −5 − +50 ’C

10) Storage Temp — −20 − +65 ’C

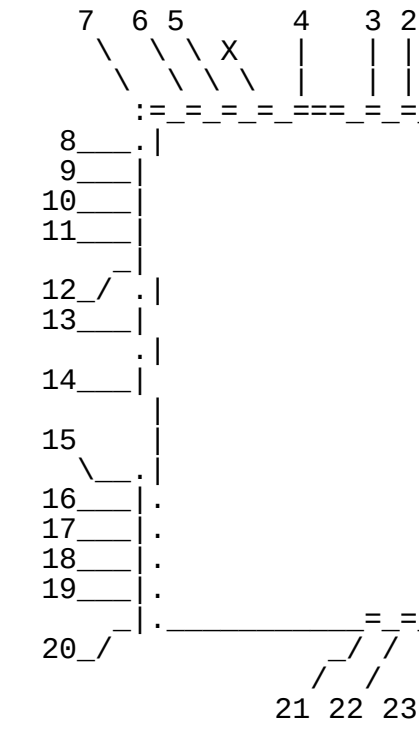
7360R7 TIMING SPECIFICATIONS ————————NTSC ONLY————————

	Single clock lo		Single clock hi		Double Clock lo		Double clock hi	
	min	max	min	max	min	max	min	max
Tcyc in	69.81	69.88						
PW in lo	25	45						
PW in hi	25	45						–
Tcyc	1117	1118	1117	1118	558	559	558	559
Clock PW	535	585	535	585	275	295	260	285
Tclkraslh	60	110	60	110	60	110		
Tclkrashl	220	260	220	260	220	260		
Tclkmuxlh	60	110	60	110	60	110		
Tclkmuxhl	260	290	260	290	260	290		
Tclkcaslh	60	110	60	110	60	110		
Tclkcasrd	300	365	300	365	300	365		
Tclkcaswr			420	470	420	470		
Traslmuxl	20		20		20			
Tmuxlcasl	35		35		35			
Traslcasl	75		75		75			
Tcaswrash	160		160		160			
Tclkcsl		305		305		305		305
Tclkcsh	40	110	40	110			40	110
Tclkaec	10	40	10	40				
PWras lo	360	440						
PWras hi	120	200						
PWcas lo	170	360						
PWcas hi	200	390						
Taddoutac		150		150				
Taddoutrl		40		40				
Tdoutstp			160				160	
Tdouthld			40	120			40	120
Tdinstp		90		90				90
Tdinhld		10		10				410
Taddinstp				400				400
Taddinhld				0				0

Approved:	Released	Rev.	Date	Engr.	Rev.	Date	Engr.	Rev.	Date	Engr.
4/19/83										

DIE SIZE: X:206 Y:198

7360R0



1: A2	25: DB0	42	
2: A1	26: DB1	41	
3: A0	27: DB2	40	
4: Vdd	28: DB3	39	
	29: DB4	38	
5: CS	30: DB5	37	
6: CSI	31: DB6	36	
7: R/W	32: DB7	35	
8: IRQ	33: SND	34	
9: MUX	34: BA	33	
10: RAS	35: AEC	32	
11: CAS	36: A15	31	
12: PhiOUT	37: A14	30	
13: Color	38: A13	29	
14: PhiIN	39: A12	28	
15: KYBD0	40: A11	27	
16: KYBD1	41: A10	26	
17: KYBD2	42: A9	25	
18: KYBD3	43: A8	24	
19: KYBD4	44: A7	23	
20: KYBD5	45: A6	22	
21: KYBD6	46: A5	21	
22: KYBD7	47: A4	20	
23: LUM/Sync	48: A3	19	
24: VSS		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		9	
		8	
		7	
		6	
		5	
		4	
		3	
		2	
		1	

Package: 48 Lead Plastic

Die Attach Area: X:290 Y:280 Scale: 20X

48 Lead bonding diagram	Page of	Specification No.

SCOPE

This specification covers the detailed requirements for a high resolution video display chip utilizing HMOS technologics. This device is intended for use in low end 6502−based personal home computer systems.

The TED chip is a 48 pin device which controls video output, system timing, dynamic RAM control, ROM chip selects, and keyboard control. The TED contains 34 control registers which are accessed through the standard 6502 microprocessor data bus. It will access up to 64K of memory for display information.

CHARACTER MODES

In any of the character modes, the TED chip displays 25 lines of 40 characters per line. Each character on the screen can be set to any of 16 possible colors, with 8 possible luminance levels.

The character pointers in the VIDEO MATRIX determine what character will be display in a particular place. Associated with each location of the video matrix is an 8 bit color memory location, called the ATTRIBUTE byte. The attribute byte determines the color, luminance level, and wether that

character will flash.

The TED chip fetches character pointers from the area of memory known as the VIDEO MATRIX area, and color information from the ATTRIBUTE area.
The video matrix consists of 1000 consecutive locations in memory, each of which contains an 8 bit character pointer. The location of the video matrix is determined by the VIDEO MATRIX BASE REGISTER in the TED (bits 3–7 of Register #20), which provides the 5 MSB of the video matrix address (A15–A11). The address A10 is always set to a 1. This gives 32 possible locations for the start of the video matrix.

The following chart makes this clear:

BASE ADDRESS	LOCATION	BASE ADDRESS	LOCATION
00000	$0400	10000	$8400
00001	$0C00	10001	$8C00
00010	$1400	10010	$9400
00011	$1C00	10011	$9C00
00100	$2400	10100	$A400
00101	$2C00	10101	$AC00
00110	$3400	10110	$B400
00111	$3C00	10111	$BC00
01000	$4400	11000	$C400
01001	$4C00	11001	$CC00
01010	$5400	11010	$D400
01011	$5C00	11011	$DC00
01100	$6400	11100	$E400
01101	$6C00	11101	$EC00
01110	$7400	11110	$F400
01111	$7C00	11111	$FC00

Each memory location in video matrix is used as a pointer to the actual character dot data which makes up the characters. The eighth (MSB) bit of each character pointers (VM7) can be interpreted in two different ways. If the RVS on bit of Ted Register 7 is a 0, the MSB of the video matrix (VM7) will determine if the character will be displayed reversed or not. If VM7 is set to 0, the character will be displayed normally. If VM7 is set to a 1, the character at that location will be displayed in reverse. Use of this feature limits the number of different character definitions to 128. If the RVS ON bit is set to a 1, the reverse feature feature is turned off, which allows the use of 256 different character definitions.

VIDEO MATRIX ADDRESS

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
VM4	VM3	VM2	MV1	VM0	1	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0

The attribute memory also consists of 1000 consecutive locations, and con–tains the FLASH bit, the 4 bits of color and the 3 bits of luminance for each character location. The location of the attribute memory is also controlled by the VIDEO MATRIX base register. Like the video matrix, the upper 5 bits of the address of the attributes are the VIDEO BASE REGISTER. However, for attribute memory, A10 is always set to a 0, so is always 1K below the video matrix. For example, if the video matrix is at $0C00, the attribute bytes are at $0800.

ATTRIBUTE MEMORY ADDRESS

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
VM4	VM3	VM2	MV1	VM0	0	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0

Each character is matrix of 8 by 8 dots, stored in the character ROM as 8 consecutive bytes. The location of this CHARACTER memory is set by CB4 to CB0

of TED Register 19. These bits are used as the 5 most significant bits of the character base address. The next 8 bits of the address of a particular character pattern come from the value of that particular location in the video matrix. (The last 3 bits come from a counter.)

CHARACTER DATA ADDRESS

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
CB5	CB4	CB3	CB2	CB1	VM7	VM6	VM5	VM4	VM3	VM2	VM1	VM0			
					CB0 (with REVERSE bit on)										

STANDARD CHARACTER MODE

In standard character mode, the character display is an 8 dot horizontal by 8 dot vertical character location formatted in 25 rows of 40 characters per row. Each character location in the video matrix has a unique color set by its attribute byte and share a common background color. Eight sequential bytes from character memory are displayed directly on the 98 lines of each character location. A ’0’ bit causes the color/luminance in background color register 0 to be used; a ’1’ bit causes the color/luminance of the associated byte of attribute memory to be displayed.

bit of character data	color source	luminance source
0	background reg 0, bits 0–3	bkgd reg 0, bits 4–6
1	attribute bits 0–3	attribute bits 4–6

MULTICOLOR CHARACTER MODE

Multicolor character mode provides additional color flexibility (up to four colors per character location) at a cost reduced horizontal resolution. Multicolor mode is selected by setting the multicolor bit (TED Register 7) to a 1. This cases the data in character memory to be interpreted in a different manner. When in multicolor mode, if bit 3 of the attribute byte is a 0 the character at that location will be displayed as normal (hires) character. If bit 3 of the attribute is a 1, that character will be displayed as a multicolor character. This allows the two character types to be mixed on a single screen. Only the first 8 colors are available as foreground colors, however. When a character is displayed in multicolor, the character data is defined as eight sequential bytes of character, with 4 dot pairs per byte. The character is displayed as a 4 by 8 dot matrix, with the horizontal dots twice as wide as in standard character mode. The dot pairs are interpreted as follows:

dot pair	color source	luminance source
00	bkgd reg 0, bits 0–3	bkgd reg 0, bits 4–6
01	bkgd reg 1, bits 0–3	bkgd reg 1, bits 4–6
10	bkgd reg 2, bits 0–3	bkgd reg 2, bits 4–6
11	attribute bits 0–2	attribute bits 4–6

Each character location can contain 4 colors, one unique to the character location, the other 3 in common with all other characters on the screen.

EXTENDED COLOR MODE

EXTENDED COLOR MODE allows the individual selection of both background and foreground colors in each character location on the screen. Each character location can select one of the 16 foreground colors and one of 4 available background registers. The character dot data is displayed as in standard color mode (with foreground color/luminance determined by the attribute for a ’1’ data bit), but the two MSB of the character pointers are used to select the background color/luminance for that screen location. Since the 2 MSB of the character pointer are in use, this means that only the first 64 character definitions in the character memory are available. (The TED chip forces A10 and A9 to 0).

BACKGROUND COLORS

Bits 6 & 7 character pointer	color source	luminance source
00	bkgd reg 0, bits 0–3	bkgd reg 0, bits 4–6
01	bkgd reg 1, bits 0–3	bkgd reg 1, bits 4–6
10	bkgd reg 2, bits 0–3	bkgd reg 2, bits 4–6
11	bkgd reg 3, bits 0–3	bkgd reg 3, bits 4–6

STANDARD (HIRES) BIT MAP MODE

In bit map mode there is a one to one correspondence between each displayed dot and memory bit. Standard bit map mode provides a screen resolution of 320 dots by 200 vertical dots. Each 8 by 8 square (corresponding to the character locations in standard character mode) can have an individually controlled background and foreground color.

The start of the bit map data area comes from the BIT MAP BASE register. The 3 bits of the bit map base are used as the A15–A13 of the address. The bit map data area is 8K, therefore bit map areas must start on 8 K boundaries.

BIT MAP BASE	ADDRESS
000	$0000
001	$2000
010	$4000
011	$6000
100	$8000
101	$A000
110	$C000
111	$E000

When in bit map mode, both the video matrix and the attribute memory are used for color data. The address of the bit mapped data is formed by combining the 3 bit BIT MAP BASE register as the MSB of the data address with the 10 bit character position counter and the 3 bit raster counter. This addressing scheme results in each 8 sequential memory locations being formated as an 8 by 8 block on the video display, something like this:

byte 0	byte 8	byte 16.....byte 312
byte 1	byte 9	byte 17.....byte 313
byte 2	byte 10	byte 18.....byte 314
byte 3	byte 11	byte 19.....byte 315
byte 4	byte 12	byte 20.....byte 316
byte 5	byte 13	byte 21.....byte 317
byte 6	byte 14	byte 22.....byte 318
byte 7	byte 15	byte 23.....byte 319
byte 320	byte 328	byte 336.....byte 632
byte 321	byte 329	byte 337.....byte 633
byte 322	byte 330	byte 338.....byte 634
byte 323	byte 331	byte 339.....byte 635
byte 324	byte 332	byte 340.....byte 636
byte 325	byte 333	byte 341.....byte 637
byte 326	byte 334	byte 342.....byte 638
byte 327	byte 335	byte 343.....byte 639

etc.

(or it could be represented like this:)

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BB2	BB1	BB0	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	VS2	VS1	VS0

When in standard bit map mode, the color information is derived from the data stored in the video matrix, while the luminance information comes from the attribute data. This allows for 2 colors to be independently selected in each 8 by 8 area. When the bit to be displayed is a '0', the color of the dot output is set by the lower 4 bits of the video matrix; the luminance is selected by bits 4–6 of attribute memory. When a bit to be displayed is a '1', the color is set by the upper 4 bits of the video matrix; the luminance is set by bits 0–2 of attribute memory.

dot	color source	luminance source
0	video matrix bits 0–3	attribute bits 4–6
1	video matrix bits 4–6	attribute bits 0–2

MULTICOLOR BIT MAP MODE

MULTICOLOR bit map mode bears the same relationship to standard bit map mode as multicolor character mode does to standard character mode. Multicolor bit map mode allows greater color selection at the cost of horizontal resolution. Using multicolor mode, up to four different colors can be displayed in each 8 by 8 bit block.

The bit map data area is addressed exactly the same as in standard bit map mode. The dot data and color information is interpreted differently, however.

Multicolor bit map mode is selected by setting both the multicolor bit and the bit map bit to '1'.

As in multicolor character mode, multicolor bit map mode uses the concept of 'dot pairs' to specify one of our pixel colors. Sinc two bits select one dot color, the horizontal resolution is halved (160H by 200V). Each multicolor pixel is twice as wide as hires pixel.

dot pair	color source	luminance source
00	bkgd reg 0, bits 0–3	bkgd reg 0, bits 4–6
01	video matrix bits 4–7	attribute, bits 4–6
10	video matrix bits 0–3	attribute, bits 4–6
11	bkgd reg 1, bits 0–3	bkgd reg 1, bits 4–6

ADDITIONAL FEATURES

Hardware Cursor

The hardware cursor is controlled by a 10 bit cursor compare register (Register 12 and 13). This allows 1024 possible positions. Setting the cursor compare register bits to a value from 0 to 999 results in the cursor appearing in the specified location (the top left corner of the screen is 0, the bottom right corner is 999, etc.). The cursor will blink at the rate of 2Hz, by switching the foreground and background colors in that location. Note: The hardware cursor can only appear during standard character mode.

Flash

The TED chip provides the ability to Flash any or all characters on the screen when using standard character mode, when the TED chip Flash bit is enabled. Flash is selected on a character by character basis, via the MSB of the attribute memory location for that character. When a character is flashing the foreground color of that character will turn off (change to background color) and on again at the rate of 2 Hz.

Dynamic Ram Refresh

Dynamic RAM refresh operation is controlled by the TED chip. Five, RAS only refreshes are performed during every raster line, immediately following

character fetches. TED guarantees a maximum delay of 3.26msec between the refresh of a single row address in a 256 address refresh scheme. This refresh is totally transparent to the system, since refresh occurs during phase one of the single speed system clock.

System Clock Doubling

For increased processor throughput, the system clock output from TED doubles frequency from 894KHz (NTSC) to 1.788KHz (NTSC), during non-display times. The horizontal position register counts 456 dots, 0 to 455. During counts of 400-344, wile in raster lines 0 to 204, the TED device outputs single clock. During this time TED is doing processor handshaking (counts 400-432), character fetches (counts 432-304), and dynamic RAM refresh (counts 304-344). Outside of this horizontal window TED outputs double clock (1.788KHz). During raster lines 205-261 for NTSC (205-311 for PAL), TED outputs double clock at all times except horizontal counts 304-344 which are single clock to allow for dynamic RAM refresh. If the blanking bit (Register #6) is cleared, the active display is cleared, the screen is filled with border color, and double clock is enabled at all times except refresh.

Sound

The TED device has two separate square wave generators. The frequency base for voices 1 and 2 are 10 bit registers (Register #24 and 18 for Voice 1 and Register #15 and 16 for Voice 2. Voice 2 can be selected to be either a square wave generator or a white noise generator. The voice selection and volume control mechanism is Register #17. There are 9 volume levels in TED, ranging from 0 being off to 8 being loud. Programming values of 9-15 in the lower nibble at this register is identical to programming the loudest, volume 8, level. Bits 4-6 of this register each individually select Voice 1, Voice 2, or white noise respectively. Voice 2 and white noise cannot be enabled together, instead Voice 2 selection will override white noise selection. The frequency generated by TED is:

$$\text{FREQUENCY} = \frac{111860.781}{(1024-x)} \quad \text{for NTSC}$$

$$= \frac{110840.45}{(1024-x)} \quad \text{for PAL}$$

A sampling frequency chart follows.

NOTE	BASE REGISTER VALUE (1028-x)	ACTUAL FREQUENCY (HZ)
A	1017	110
B	906	123.5
C	855	130.8
D	762	146.8
E	679	164.7
F	641	174.5
G	571	195.9
A	508	220.2
B	453	246.9
C	428	261.4
D	381	293.6
E	339	330
F	320	349.6
G	285	392.5
A	254	440.4
B	226	494.9
C	214	522.7
D	190	588.7
E	170	658
F	160	699
G	143	782.2

A	127	880.7
B	113	989.9
C	107	1.045K
D	95	1.177K
E	85	1.316K
F	80	1.398K
G	71	1.575K

Internal Operation

All internal timing operations are based on the horizontal dot counter. Particular events occur in response to certain counts of both the horizontal position register and the vertical line register.

HORIZONTAL DECODES			HORIZONTAL COUNT
Horizontal Sync	Start		358
	Stop		390
Horizontal Equalization Pulse 1	Start		152
	Stop		170
Pulse 2	Start		380
	Stop		398
Horizontal Blanking	Start		344
	Stop		416
Burst	Start		384
	Stop		408
Character Windows	Start		432
	Stop		296
External Fetch Window	Start		400
	Stop		288
Refresh Single Clock	Start		288
	Stop		328
Character Window Single Clock	Start		432
	Stop		296
40 Column screen	Start		451
	Stop		315
38 Column screen	Start		3
	Stop		307
Video Shift Register	Start		440
	Stop		304
Increment Blink			336
Increment Vertsub Counter			
Increment Refresh	Start		296
	Stop		336
Increment Character Position Reload			424
Increment Character Position	Start		432
	Stop		288
Latch Character Position to Reload			290
End of Screen – Clear Vertical Line, Vertical Sub and Character Reload Registers			384
Increment Vertical Line			376

Many of the events are qualified by a vertical line count.

VERTICAL DECODES		VERTICAL COUNT
End of Screen PAL		311
End of Screen NTSC		261
Vertical Sync PAL	Start	254
	Stop	257
NTSC	Start	229
	Stop	232
Vertical Equalize PAL	Start	251
	Stop	260
NTSC	Start	226
	Stop	235
Vertical Blanking PAL	Start	251
	Stop	269

	NTSC	Start		226
		Stop		244
Attribute Fetch	Start			0
	Stop			203
Frame Window	Stop			204
Vertical Screen Windows	25 Row	Start		4
		Stop		204
	24 Row	Start		8
		Stop		200

TED REGISTER DESCRIPTION

Internal Timers, Register 0 through 5

Ted contains three 16 bit decrementing interval timers, each partitioned into 2, 8 bit registers. To initiate a new count value, loading the low Byte inhibits counting until the high Byte is loaded. The timers decrement at a 894 KHz rate for NTSC television systems, 884 KHZ for PAL systems. Each counter generates an interrupt upon decrementing to 0. The sequence for writing to the timers should be:

Disable all interrupts
Write low Byte
Write high Byte
Enable desired interrupts

Care should be taken that long time intervals, more than 125u seconds, do not occur between writing the low and then the high Bytes.

Timer 1 is a sequence interval timer. Registers 0 and 1 when written to initiate the reload value of the timer. When timer 1 is decremented to 0, the next count occurs from the reload value. Reading Registers 0 and 1 gives the current count valve.

Timers 2 & 3 are free running counters. Upon decrementing to 0 the timers roll over to FF and continue counting. Writing to timer 2 and 3 registers loads directly into the active count. Reading these registers yields the current count.

Register 6

Bits 0–2 of this register determine the vertical scroll position. For a normal 25 row picture with no scroll these bits should be a ’3’. Bit 3 is the 24/25 row select. A ’0’ in this both corresponds to 24 rows and a ’1’ yields 25 rows. For vertical scroll to occur, bit 3 should be cleared and bits 0–3 all set. Decrementing bits 0–2 moves character position up scrolling off the uppermost character row. Bit 4 is the blanking bit. Setting this bit to a ’1’ gives a normal picture. Setting it to a ’0’ blanks the screen and disables all fetches from occurring, allowing for the system clock to run at twice the frequency (1.788MHZ NTSC, 1.768MHZ for PAL) except for 5 refresh cycles per raster line. Bits 5 and 6 are display mode Bits. Setting Bit 5 to a ’1’ enables Bit mapped mode, while setting bit 6 enables extended color mode. Bit 7 is a bit used for I.C. testing and must remain a ’0’.

Register 7

Bits 0–2 determine the horizontal scroll position. A ’0’ in these bits allows for no scroll. To institute scroll bit 3 of this register, the 38/40 column bit, should be set to ’0’. This displays 38 columns and scroll can occur cleanly. Incrementing the 3 LSB of this register pans the character positions to the right.

Bit 4 is multicolor mode bit. Setting this bit to ’1’ enables multicolor. The freeze bit is bit 5. Setting freeze high stops TED from incrementing the horizontal position, the timers and the vertical position. The system is forced into single clock (894KHZ) and system refresh of dynamic rams. Bit 6 is PAL/. Setting this bit high forces NTSC mode, low corresponds to the PAL mode. Bit 7 is the reverse video off bit. Under normal condi–

tions, bit 7=0, there are 128 character locations. The reverse video character is implemented by setting the MSB of the video matrix pointer to a '1'. This enables the TED chip to invert the character data and thus reverse video. If an alternate character set of 256 locations is desired, this bit can be set high turning the reverse video feature off and allowing the the MSB of the video matrix to define the additional character locations.

Register 8

This register is the keyboard latch. Writing to Register 8 scans the keyboard lines and latches the appropriate data. Reading the register, reads the latched data.

Register 9

The interrupt register indicates any TED interrupt source. Possible interrupt sources are:

Bit 1 raster interrupt –compares raster register to active count
Bit 3 timer 1 interrupt –timer 1 has decremented to '0'
Bit 4 timer 2 interrupt – " 2 " " " " "
Bit 6 " 3 " " – " 3 " " " " "

Bit 2 indicates a light pen interrupt. The TED computer does not have light pen. This bit is for future expansion. Bit 7 is the interrupt bit. It is the inversion of the interrupt pin. Writing a '1' to the interrupt register clears the individual interrupt bit.

Register 10

Register 10 is the interrupt mask register. The individual mask bit corresponds to each of the possible interrupt sources. Setting the bit high enables interrupts to occur. The LSB of this register is the MSB of the raster register. (see Register 11 description)

Register 11

In an NTSC television system. 262 raster lines are produced (0 to 261), 312 for PAL (0–311). To detect all possible raster lines a 9 bit register is needed. Register 11 contains the low order 8 bits of this raster register. Register 10 contains the MSB. The raster register is an interrupt source. The raster register value is compared to the current vertical line count. An interrupt is generated 8 cycles before the character window. For a 25 row display, the visible raster lines are from 4 to 203.

Register 12

Register 12 contains the 2 MSB of the cursor position register. Bits 0 and 1 correspond to the cursor bits 8 and 9.

Register 14

Register 14 contains the low byte of Voice 1 frequency base. All TED sound generators produce square waves.

Register 15

The low order eight bits of the frequency base for the second voice source are contained in this register. This voice is selectable for either white noise or another square wave generator. This selection is available in Register 17.

Register 16
This registers contains the 2 MSB of Voice 2.

Register 17
has 4 bits of volume control ranging from 0 = OFF to '8' being

loud. Also 3 voice selects are available. Voice 1 select, Voice 2 square wave select and Voice 2 white noise select. The MSB of this register is a bit used for testing. The sound reload bit will clear the sound toggle flops and initiate the reload value of each voice to initialize the active sound count during the appropriate voice incrementing time. This bit will also initiate the white noise random number generator to ’1’s.

Register 18

This register contains the three bit bit map mode address base, the ROM/RAM bank bit, and the 2 bit MSB of voice 1 frequency base. The bit map base determines where in the memory map the bit map dot data can reside. Bits 3 through 5 correspond to BMB0 to BMB2. During TED dot fetches in the bit map mode, BMB2 will become A15, BMB1 − A14, and BMB0− A13. The ROM/RAM bank bit, bit 2, will force TED dot and character fetches from either ROM or RAM. A ’1’ in this bit will force ROM execution a ’0’ will force RAM.

Register 19

This register contains the character base, force single clock bit, and the status bit. The force single clock bit, when set high, inhibits the PH out of TED from doubling frequency during horizontal blanking. The status bit is a read only bit indicating the state of the 2 phantom Registers 62 and 63. If this bit is high it indicates that TED is operating for the ROM bank memory. This bit does not indicate where TED will fetch character or dot information is coming from.

Register 20

The 5 bit video matrix base, bits 3 through 7, comprise Register 20. The video matrix base determine the memory mapping of the video matrix pointers and the attribute data as shown:

A15	A14	A13	A12	A11
VM4	VM3	VM2	VM1	VM0

The attribute and video matrix fetches occur on the raster line preceding the character row (attribute) and the first raster line of the character row. During these fetches TED will DMA the processor and take complete control of the system bus for both halves of the clock cycle, for 40 consecutive clock cycles.

Register 21

This register contains a three bit luminance code and a four bit color code for background Register 0. This allows for eitht separate luminance level for each 16 colors.

Register 22
contains the same data as Register 21 for background Register 1.

Register 23
Background Register 2 data is stored here.

Register 24
is comprised of luminance and color data for background Register 3.

Register 25
Luminance and color information for the exterior register (border) is stored in Register 25.

Register 26

The two MSB of the character position reload register are bits 0 and 1 of this register. The character position reload increments by forty each character row completed. For example, during the first character row this register will contain ’0’. Upon completion of the eighth raster line of the row, the character position bit map reload register will be updated to 40.

Register 27
The low byte of the character position reload register is located here. (See Register 26).

Register 28

This register contains only 1 bit, the MSB of the vertical line register. The vertical line register contains the current raster line being displayed. For NTSC systems this register will count from 0 to 261, for PAL, 0 to 311.

Register 29
The low byte of the vertical line register is contained in Register 29.

Register 30

Register 30 is the horizontal position register. Register 30 contains the upper 8 bits of this nine bit register. The LSB increments at a rate too fast to be of any use in programming. Since the horizontal position register actually increments from 0 to 455, Register 30 will contain values of 0 to 228. Negative true data is to be written to this register while positive true data is read.

Register 31
This register contains the 4 bit blink rate register and the 3 bit vertical subaddress register. The blink rate register contains the current count of the blink rate times. This register is incremented once per screen. On overflow a 2HZ signal is generated initializing the cursor reverse video and any flashing characters. The vertical subaddress counts the eight raster line per character row.

Register 62 and 63

These registers do not physically exist on the TED chip. A write to these locations controls the TED system memory map. Any write to Register 62 results in ROM being selected in memory locations $8000(HEX) to $FFFF(HEX) excluding $FD00(HEX) to $F3FF(HEX) for I/O space and TED space. The TED chip will generate the necessary chip selects and inhibit CAS until a write to Register 63 occurs. Upon this occurrence, the same locations $8000(HEX) to $FFFF(HEX) excluding $FD00(HEX) to $F3FF(HEX) are banked to RAM. CAS occurs when appropriate and chip selects are suspended.

All TED registers, unless otherwise noted, are read/write. It should be noted that care should be taken when writing to Register 26 through 31. These are internally controlled registers. Writing to them can result in a flicker on the screen.

PINOUT

PIN #	DESIGNATION	SIGNAL DIRECTION	SIGNAL POLARITY	DESCRIPTION
1	A2	input/output	+true	address bit 2
2	A1	"	"	" 1
3	A0	"	"	" 0
4	VDD	input	5V	power supply
5	CS0	output	−true	low ROM chip select
6	CS1	output	"	high ROM chip select
7	R/W	input/output	+true	read/write
8	IRQ	output	−true	interrupt
9	MUX	output	"	address multiplex switch
10	RAS	"	"	RAM row address strobe
11	CAS	"	"	RAM column address strobe
12	0out	"	"	894.9KHz CPU clock (NTSC) 886.7KHz CPU clock (PAL)
13	COLOR	"	+true	chrominance
14	0in	input	"	14.31818MHZ single phase

				+/−10% (NTSC)
				17.734475MHZ single phase
				+/−10% (PAL)
15	K0	input/int pullup	"	keyboard latch 0
16	K1	" " "	"	" 1
17	K2	" " "	"	" 2
18	K3	" " "	"	" 3
19	K4	" " "	"	" 4
20	K5	" " "	"	" 5
21	K6	" " "	"	" 6
22	K7	" " "	"	" 7
23	LUM	output	"	composite sync and luminance
24	VSS	input	0V	power supply
25	DB0	input/output	+true	data bit 0
26	DB1	" "	"	" " 1
27	DB2	" "	"	" " 2
28	DB3	" "	"	" " 3
29	DB4	" "	"	" " 4
30	DB5	" "	"	" " 5
31	DB6	" "	"	" " 6
32	DB7	" "	"	" " 7
33	SND	output	+true	sound
34	BA	output	+true	bus available
35	AEC	"	"	tri−state control
36	A15	input/output	"	address bit 15
37	A14	" "	"	" " 14
38	A13	" "	"	" " 13
39	A12	" "	"	" " 12
40	A11	input/output	+true	address bit 11
41	A10	" "	"	" " 10
42	A9	" "	"	" " 9
43	A8	" "	"	" " 8
44	A7	" "	"	" " 7
45	A6	" "	"	" " 6
46	A5	" "	"	" " 5
47	A4	" "	"	" " 4
48	A3	" "	"	" " 3

PIN FUNCTIONS

ADDRESS BUS pins 1 thru 3 and 36 thru 48
The 16 bit address bus is bidirectional. As an input, the microprocessor can access any of the 34 TED control registers. In the output mode TED uses the addresses to fetch Video Matrix Pointers, Attribute Pointers or character cell information. For microprocessor interface TED resides in locations FF00−FF3F in memory.

DATA BUS pins 25 thru 36
The 8 bit data bus is also bidirectional. The data bus activity can be separated into 2 categories: microprocessor interface and video data interface during the above mentioned fetches.

KEYBOARD LATCH pins 15 thru 22
The 8 bit keyboard latch is used as the keyboard interface. Upon an instruction by the microprocessor to write to the keyboard latch, the information on the keyboard pins is latched by TED and stored until it is retrieved by the microprocessor on a read keyboard instruction. The keyboard pins also provide the active pull up on the keyboard matrix lines. These pull ups source a minimum 600u amps and maximum 900m Amps current. The trip point of the keyboard latch is 2.0 Volts.

Two of the keyboard pins also provide testing functions. When these pins are externally driven to 10 volts, they provide specific testing features. K0 generates a system freeze function, stoping the horizontal counter, thus freezing the position, and sets all horizontal flip−flops to force TED into the dynamic RAM refresh period and single clock. All flip−flops are then released to allow their manipulation by the horizontal register. K1 forces

the internal clock division into the NTSC mode.

CHIP SELECTS pins 5 and 6
Ted generates ROM chip selects based on address decoding. CS0 is active during the memory block of 8000−BFFF (HEX). CS1 corresponds to C000−FFFF (HEX) in memory. The ROM area of memory can be banked out to overlay RAM, see the descriptions of Registers 3E and 3F (HEX).

DYNAMIC RAM CONTROL pins 9 thru 11
TED generates RAS and CAS for dynamic RAM access. The signal MUX is also generated to externally multiplex the RAM row and column addresses.

READ/WRITE pin 7
R/W is an input to TED to distinguish the type of operation to be performed. TED will actively pull up the system read line during all TED fetches. The read signal is qualified with MUX. The pon is an open source output.

INTERRUPT pin 8
The interrupt pin is an open drain output. TED contains four interrupt sources: 3 internal timers and the raster comparator.

PHI OUT pin 12
For increased processor throughput, TED doubles the frequency of the system clock during horizontal and vertical blanking. The actual single clock boundaries are:

1) raster lines 0−204 and horizontal positions 400−344
2) horizontal positions 304−344

PHI IN pin 14
For use in NTSC television systems, TED requires a 14.31818 MHZ single phase clock input. For PAL systems, the input clock must be 17.734475MHZ single phase.

COMPOSITE COLOR pin 13
The color output contains all chrominance information, including the color reference burst signal and the color of all display data. The color output is open source and should be terminated with 1K ohms to ground.

COMPOSIT SYNC AND LUMINANCE pin 23
The luminance output contains all video synchronization as well as luminance information of the video display. This pin is open drain, requiring an external pullup.

SOUND pin 33
This pin provides the output of the 2 tone generators. The output must be integrated through an RC network and then buffered to drive an external speaker.

BUS AVAILABLE pin 34
Bus Available indicated the state of TED with respect to video memory fetches. BA will go low during phase 1, 3 single clock cycles before TED performs any memory access and will remain low for the entire fetch.

ADDRESS ENABLE CONTROL pin 35
During double clock mode, AEC is always high allowing the 6510 complete control of the system buses. For single clock time periods, when BA has not gone low, AEC will toggle with 02out. This allows TED PHi1, time to complete its memory accesses of video dot information while the 6510 performs during Phi2. When TED needs both halves of the cycle to perform it customary Phi1 dot fetches and Phi2 attribute and pointer fetches, BA will go low. On the fourth Phi1 out, AEC will remain low until the end of the Phi2 video fetch.